EXHIBIT 28

.UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

SOLAS OLED LTD., an Irish corporation, Plaintiff, v. LG DISPLAY CO., LTD., a Korean corporation; LG ELECTRONICS, INC., a Korean corporation; and SONY CORPORATION, a Japanese corporation, Defendants.	**CASE NO. 6:19-CV-00236-ADA** **JURY TRIAL DEMANDED**

RESPONSIVE DECLARATION OF DOUGLAS R. HOLBERG

I, Douglas R. Holberg, make this declaration in support of Defendants' Responsive Claim Construction brief. Any statements I make below based on my own knowledge are true, and based on information and belief are believed to be true. The opinions stated herein are my own.

1. I am more than eighteen years of age, and I am a citizen of the United States, currently residing in Texas.

2. I have been retained by counsel for Defendants to provide my opinions as to the meaning of certain terms in the asserted claims of U.S. Patent Nos. 7,907,137 (the "'137 patent"), 7,432,891 (the "'891 patent"), and 7,573,068 (the "'068 patent"), asserted by Solas OLED Ltd. ("Solas") in this action (collectively, the "Asserted Patents"). I previously submitted a declaration entitled Declaration of Douglas R. Holberg (Dkt. 67-2) relating to claim construction issues, which I incorporate by reference here.

3. I understand that Solas submitted a Declaration of Richard A. Flasck in Support of Solas's Opening Claim Construction Brief (Dkt. 68-2, "Flasck Decl."). I have reviewed that declaration. In response to certain issues that were raised by Mr. Flasck, I have expanded on the opinions in my opening declaration as set forth below. My opinions below should be read together with and in light of the opinions in my opening declaration.

4. This declaration is based on information currently available to me. I understand that claim construction proceedings are still ongoing, and I reserve the right to expand or modify my opinions as my investigation and study continues. I may also supplement my opinions in response to any additional information that becomes available to me, any matters raised by Solas and/or any opinions provided by Solas and/or opinions provided by Solas's expert(s), or in light of any relevant orders from the Court.

5. For the purposes of preparing this declaration, I have reviewed the Mr. Flasck's declaration and the documents he cites, as well as the documents referred to in my opening declaration.

6. In forming my opinions, I have considered the documents identified in my opening declaration and below, and my knowledge and experience based upon my work in the field of the patents in suit as described in my opening declaration.

7. In his declaration, Mr. Flasck opines that the specification of the '068 patent uses the term "patterned together" to mean "the spatial sense of patterned to fit together, not the temporal sense of patterned at the same time." I disagree. In particular, Mr. Flasck focuses on the following highlighted sentence from the specification of the '068 patent.

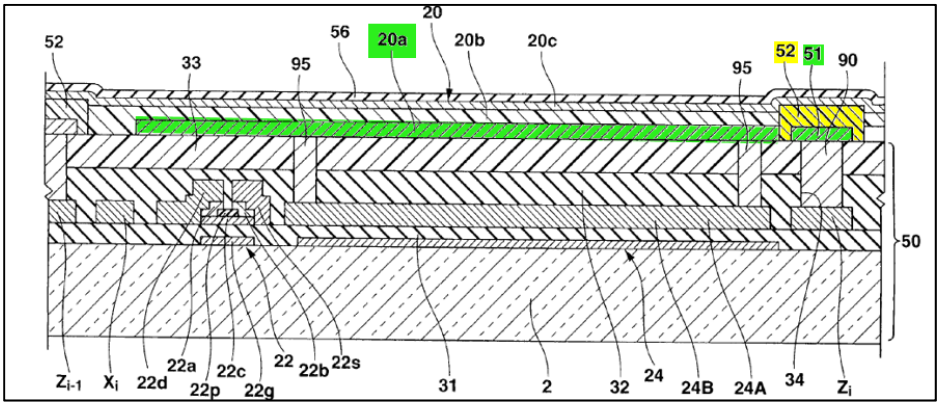
> The pixel electrodes **20***a* are formed, using photolithography and etching, by patterning a conductive film (a transparent conductive film for a bottom emission type) formed on the entire surface of the planarization film **33**. On the feed interconnections **90** between the pixel electrodes **20***a* adjacent in the vertical direction, conductive lines **51** electrically connected to the feed interconnections **90** along them are patterned on alternate columns of the pixel electrodes **20***a*. The conductive lines **51** are patterned together with the pixel electrodes **20***a* by etching a conductive film as the prospective pixel electrodes **20***a*. The width of each conductive line **51** is so larger than that of the feed interconnection **90** under it that the feed interconnection **90** is covered not to expose and protected from the etchant of the conductive lines **51**.

'068 patent at 11:4-17; *see* Flasck Decl. ¶ 124 (citing '068 patent at 11:11-14).

8. In the highlighted sentence above, the specification states that the "conductive lines 51" and the "pixel electrodes 20a" are patterned together. What those two electrical components are formed from is a "conductive film as the prospective pixel electrodes 20a." In other words, the conductive film that is deposited and will be used to form the pixel electrodes 20a (a

"conductive film as the prospective pixel electrodes 20a") is patterned by etching to form, at the same time and in the same step, the pixel electrodes 20a and the conductive lines 51.

9. Figure 8 confirms this understanding. As I have shown in the annotated version below, elements 20a and 51 are formed from the same single conductive film, colored green, indicating that they were formed at the same time by photolithography and etching. Moreover, Figure 8 confirms something that would be obvious to a person of ordinary skill in the art: elements 20a and 51 do not "fit together." Instead, they are isolated from each other by a "mesh-shaped insulating film 52 made of insulating material such as silicon nitride." '068 patent at 11:18-20.



'068 patent at Fig. 8 (annotated).

10. Contrary to the above, Mr. Flasck contends that the highlighted sentence above from the '068 patent at 11:11-14 refers to "etching a film for 'prospective' (future) pixel electrodes 20a [which] ensures that the conductive lines will fit together when the actual electrodes are formed" as Mr. Flasck opines. Flasck Decl. ¶ 124. Mr. Flasck appears to rely heavily on the word "prospective" out of context of the sentence itself and the '068 patent as a whole, suggesting that it implies some future step or state of fitting together. The relevant phrase, however, is not "prospective pixel electrodes 20a" alone, but rather a "conductive film as the prospective pixel electrodes 20a." That "conductive film as the prospective pixel electrodes 20a" refers to the conductive film, before it is patterned, that will form the pixel electrodes as discussed above.

11. The first sentence of the paragraph where the "conductive film as the prospective pixel electrodes 20a" language appears refers to the pixel electrodes 20a being formed by patterning "a conductive film … ***formed on the entire surface*** of the planarization film 33." In other words, before patterning, the conductive film is deposited as a thin film with a uniform thickness over the entire surface of the wafer, as it conventionally done in integrated circuit manufacturing. Until that deposited film is patterned, it does not form any actual electrical components; it is simply a conductive film that prospectively (i.e. in the future) will form components after it has been patterned. Then, as a result of patterning the layer by photolithography and etching, the actual components in that layer are formed at the same time, i.e., "patterned together."

12. The rest of the specification also supports that the term "prospective" above refers to the unpatterned film, from which actual components will be formed at the same time (i.e., simultaneously) through patterning.

13. Below is one such example from the "Description of the Related Art."

> In the conventional organic electroluminescent display panel of active matrix driving type, interconnections such as a power supply line to supply a current to an organic EL element are patterned simultaneously in the thin-film transistor patterning step by using the material of a thin-film transistor such as a switching transistor or driving transistor. More specifically, in manufacturing the display panel, a conductive thin film as a prospective electrode of a thin-film transistor is subjected to photolithography and etching to form the electrode of a thin-film transistor from the conductive thin film. At the same time, an interconnection connected to the electrode is also formed. For this reason, when the interconnection is formed from the conductive thin film, the thickness of the interconnection equals that of the thin-film transistor.

'068 patent at 1:57-2:4.

14. This paragraph explains that in conventional OEL display panels, interconnections and TFT electrodes can be "patterned simultaneously" using the material of a TFT. The next sentences go on to explain that what this means "[m]ore specifically" is that "in manufacturing the display panel, ***a conductive thin film as a prospective electrode*** of a thin-film transistor is subjected to photolithography and etching to form the electrode of a thin-film transistor" ***and*** "***[a]t the same time***, an interconnection connected to the electrode is also formed." In other words, "prospective" is used to refer to the electrode that will be created for a thin film transistor from an unpatterned conductive thin film ***after*** it has been patterned by photolithography and etching. The final sentence of the above also clarifies that, because the TFT electrodes and the interconnects (i.e., supply lines) are formed from the same conductive film at the same time, the components have the same thicknesses.

15. Another example of the specification's use of the word "prospective" is with reference to a "protective film 35a formed by patterning a film as the ***prospective*** semiconductor films 23c is provided on each of the signal lines Y_1 to Y_n.". '068 patent at 25:17-20. As shown in Figures 23 and 24, elements 35a and 23c are formed in the same layer together, at the same time, as part of the same patterning step. *Id.* at Figs. 23, 24.

16. Mr. Flasck also contends that prior art U.S. Patent No. 7,250,722 (Dkt. 68-16, the "'722 patent") uses the term "patterned together" to mean "patterned to fit together." Flasck Decl. ¶ 126. I disagree. It uses the term to mean patterned at the same time. The '722 patent uses "patterned together" in the following sentence describing Figure 8: "A first reflective electrode 294 will be patterned together with first 296 and second 298 connectors for the second 304 and third 308 electrodes." '722 patent at 18:32-35.

17. It is immediately apparent to one of ordinary skill in the art from Figure 8 that elements 294 and 296 are patterned together, at the same time, as part of the same layer because the figure represents these elements as having the same cross hatching pattern (as is conventional), the specification describes them as being conductive materials, and they are described as being patterned together. However, one of ordinary skill in the art would have understood that the cross hatching in the Figures shown in the '722 patent are not entirely reliable as certain elements include clear draftsmen's errors, and thus the cross hatching cannot be viewed in isolation from the written description as teaching what constitutes the layer used to form a component (or components) of the device. For example, Mr. Flasck points to a clear draftsman's error where a third element 298 is shown in Figure 8 as having a different cross hatching pattern than elements 294 and 296, which the written description describes as being patterned together with element 298. A POSITA would have understood that the cross hatching of element 298 cannot be correct, because if it were, element 298 would be the same material as elements 188 and 300 which are described as being formed from dielectric materials. *Id.* at 18:30-32 ("dielectric materials 300 will be formed to ***insulate the electrodes from each other***."). Element 298, however, is a "connector" that is formed "for an electrode" to allow electrical signals and thus a POSITA would understand that element 298 must be a conductive material (like elements 294 and 296 that it is patterned together with). If element 298 were instead a dielectric material, it would ***insulate*** the electrode it is formed on top of, rather than "connecting" it.

18. I also confirmed that the different cross hatching of element 298 is mistaken by looking to the other embodiments of the patent. For example, Figure 3 shows another embodiment with elements 154, 144, and 102 that are the same as elements 296, 294, and 298, respectively, in Figure 8, and are similarly "patterned together." And in Figure 3, those elements are each shown

having the same cross hatching, which is consistent with the written description that describes the elements as being formed together by patterning.

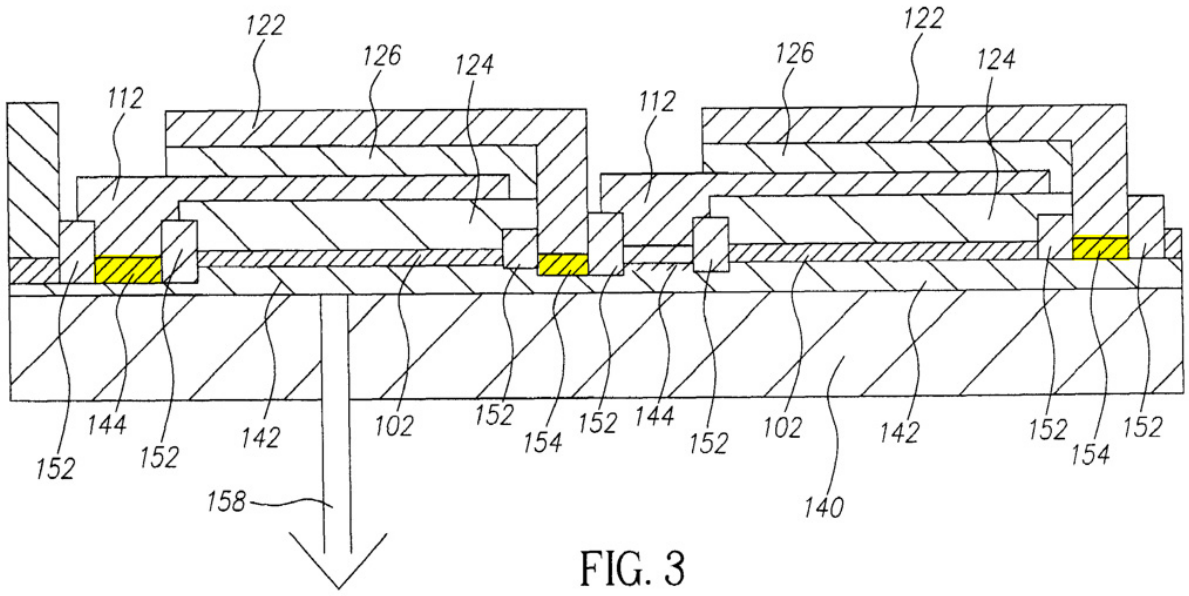


FIG. 3

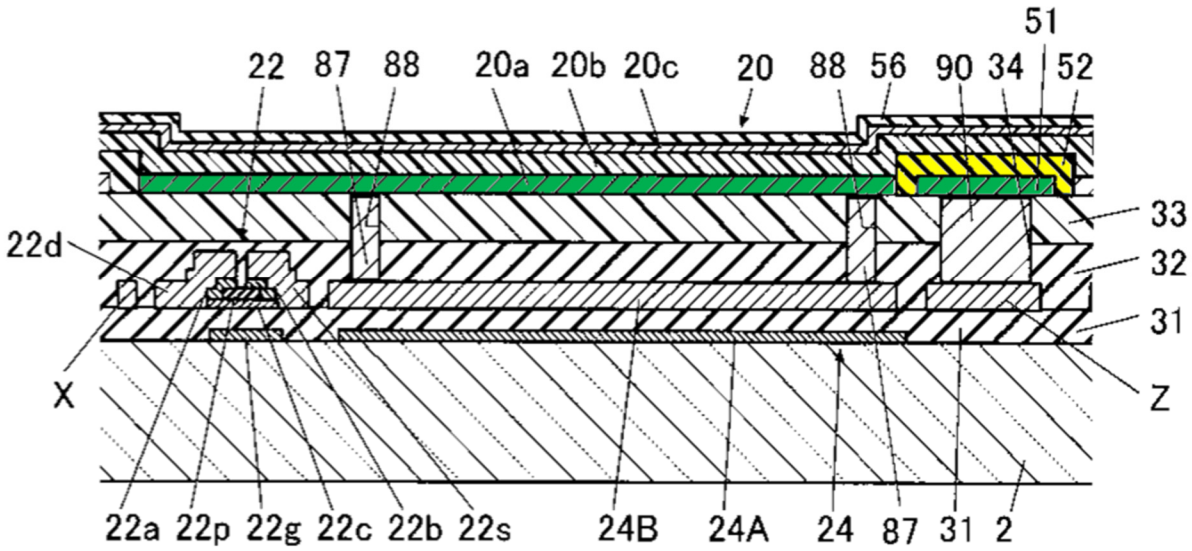
'722 patent at Fig 3[1]; *see also id.* at 12:65-13:14 ("the first electrode 102 will be patterned…a first connector 144 … will also be formed … a second connector 154 … will also be formed.").

19. A POSITA would have understood that the '722 patent's disclosure of "patterned together" is entirely consistent with the usage of that term in Solas's '068 patent, which is to describe a single layer of material that is patterned to form multiple components at the same time using photolithography and etching. While the artist who prepared Figure 8 of the '722 patent mistakenly used different cross hatching for element 298, this error does not change my opinion that patterned together in this context means patterned at the same time.

[1] Element 144 is also identified a second time in the center of Figure 3, but the cross hatching is wrong, extends past the relevant box, and the line connecting the number 144 is to the wrong element. This also demonstrates that, generally, the cross hatching in the Figures is unreliable in the '722 patent.

20. Other prior art from Casio Computer Co. Ltd., which I understand was the original assignee of the '068 patent, confirms my opinion that the term "patterned together" in the '068 patent's claims refers to components that are formed by patterning a single layer of material at the same time. For example, Japanese Patent JP 2006-100727A (Ex. 33[2], the "JP727 patent") originally assigned to Casio Computer Co. Ltd., who I understand was the original assignee of the '068 patent, used the phrase "patterned together with" to refer to electrical components that are formed at the same time by etching a single conductive film in a similar fashion to Fig. 8 of the '068 patent. Specifically, with reference to Figure 7, the JP727patent discloses a "conductive line 51 ***is patterned together with*** the sub-pixel electrode 20 a by etching the conductive film which is the source of the sub-pixel electrode 20 a." JP727 ¶ 65. As shown in annotated Figure 7 below, conductive line 51 and sub-pixel electrode 20a are formed in the same layer, with the same cross hatching, and therefore at the same time. And just like Figure 8 of the '068 patent discussed above, these components that are "patterned together" do not at all "fit together." Rather, they are insulated from one another by insulating film 52.

[2] All exhibits are to the Declaration of Blake R. Davis in Support of Defendants' Responsive Claim Construction Brief.

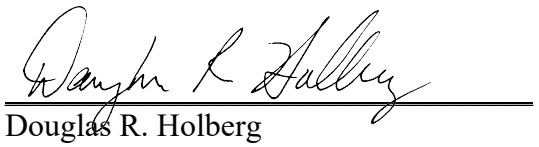


JP727 patent at Fig. 7 (annotated).

21. As another example, U.S. Patent No. 7,317,429 (Ex. 34, the "'429 patent") was originally assigned to Casio Computer Co., Ltd., names a common inventor with the '068 patent (Tomuyuki Shirasaki), and is cited as prior art to the '068 patent. *See* '429 patent at Cover; '068 patent at Cover. The '429 patent describes that when multiple circuit components, like the conductive lines and TFT electrodes of the '068 patent claims (i.e., "supply lines patterned together with the sources and drains"), are formed by patterning a single metal layer, the patterning is performed in the "same step," i.e. at the same time. *See, e.g.,* '429 patent at 7:64-8:3 (depositing "a metal film" that is "***patterned to form*** the gate electrodes of the transistors 10, 11 and 12, the selection scan lines X_1, X_2, . . . , X_m, and the emission voltage scan lines Z_1, Z_2, . . ., Z_m in ***the same step***."), 8:8-14 ("a metal film deposited on top of these components is ***patterned to form*** a source electrode 10S and drain electrode 10D of the transistor 10, a source electrode 11S and drain electrode 12D of the transistor 11, a source electrode 12S and drain electrode 12D of the transistor 12, and current lines Y_1, Y_2, . . . , Y_n ***in the same step***.").

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements are punishable by fine or imprisonment, or both, under Section 101 of Title 18 of the United States Code.

I declare under penalty of perjury that the foregoing is true and correct.



Douglas R. Holberg

3 April 2020

Date